IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/332,271
Confirmation No. ..... None
Filing Date ..... June 11, 1999
Inventor ..... Klaus Florian Schuegraf et al.
Assignee ..... Micron Technology, Inc.
Group Art Unit 2812
Examiner ..... Ron E. Pompey
Attorney's Docket No. MI22-532
Customer No. 21567
Title: Methods for Forming Wordlines, Transistor Gates, and Conductive Interconnects, and Wordline, Transistor Gate, and Conductive Interconnect Structures

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References -- See Attached Form PTO-1449

The attached form PTO-1449 is submitted in compliance with 37 CFR §1.56. No admission is made regarding whether any of the submitted references is prior art. Copies of the references are attached.

Respectfully Submitted:

Dated: 8/28/03

Robert C. Hyta
Reg. No. 46,791

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Form PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

LIST OF ART CITED BY APPLICANT

(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
M122-532	09/332,271
APPLICANT: Klaus Florian Schuegraf et al.	
FILING DATE: June 11, 1999	GROUP: 2812

U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

	AN		Ohnishi, K. et al., *Improving Gate Oxide Integrity (GOI) of a W/Wnx/dual-poly Si Stacked-Gate by Using Wet-Hydrogen Oxidation in 0.14-*
			μm CMOS devices, IEDM, 1998, pgs. 397-400.
	AO		Kawada, K. et al., *Water Vapor Generator By catalytic Reactor*, pgs. 10-16.
	AP		Wakabayashi, H. et al., *An Ultra-Low Resistance and Therma Stable W/pn-Poly-Si Gate CMOS Technology using Si/TiN Buffer Layer*,
			IEDM, 1998, pgs. 393-396.
			Hiura, Y. et al., *Integration Technorology of Polymetal (W/WSiN/Poly-Si) Dual Gate CMOS for 1 Gbit DRAMs and Beyond*, IEDM, 1998,
			pgs. 389-392.
			Nagahama, T. et al., *Wet Hydrogen Oxidation System for Metal Gate LSI's*, pgs. 140-143
			Lee, B. et al., *In-situ Barrier Formation for High Reliable W/barrier/poly-Si Gate Using Denudation of WN_x on Polycrystalline Si*, IEDM,
			1998 pgs. 385389.

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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